Anshu Gupta

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Summary

Third-year Ph.D. student in Computer Engineering with experience in hardware-software co-design and high-performance computing focused on accelerating bioinformatics workflows. Skilled in C, C++, Python, Verilog, SystemVerilog, R, and High-Level Synthesis, I am seeking research opportunities to leverage my expertise in similar fields.

Education

University of California San Diego **September 2022 – Present**
Ph.D. student in Computer Science and Engineering *La Jolla, CA*

University of California San Diego **September 2022 – June 2024**
Masters in Computer Science and Engineering; GPA - 4/4 *La Jolla, CA*

Indian Institute of Engineering Science and Technology, Shibpur **July 2015 – May 2019**
B.Tech. in Electronics and Telecommunication Engineering; GPA - 9.55/10 (Rank: 4) *West Bengal, India*

Technical Skills

Programming Languages: Verilog, SystemVerilog, Python, C/C++, R
HPC & GPU Tools: CUDA, MPI, OpenMP, Intel TBB
Software tools: Vitis HLS, Vivado Design Suite, Synopsys SpyGlass, Cadence SimVision
Cloud & Workflow Management: Amazon AWS, Snakemake, Slurm, Git, Bash

Work Experience

Analog Devices, Inc. **June 2023 – September 2023**
ASIC BU Digital Design Intern *Wilmington, Massachusetts*

- Conducted hardware architectural benchmarking for Cadence Tensilica Xtensa configurable processors.
- Characterized performance, power, and area metrics for optimal low-power embedded processor configurations.

Analog Devices India Pvt. Ltd. **July 2019 – July 2022**
Digital Design Engineer *Bengaluru, India*

- Optimized radar signal processing algorithms for automotive radar-based SoC using SIMD operations, reducing DSP cycle count by 33%.
- Contributed to the digital front-end design and tape-out of low-power Battery Management Systems SoC.
- Conducted quality assurance tasks (Lint, Clock/Reset Domain Crossing (CDC/RDC), Logic Equivalence Checks (LEC)) for BMS SoC RTL design, ensuring design integrity.
- Evaluated ARM Cortex-M processor architecture and SRAM/ROM architecture's power, performance, and area trade-offs for low-power embedded SoCs.

Research Experience

University of California San Diego **November 2022 – Present**
Graduate Student Researcher (Advisor: Prof. Yatish Turakhia) *La Jolla, CA*

- **Developed** DP-HLS, an open-sourced HLS-based framework, to flexibly accelerate dynamic programming(DP)-based bioinformatics algorithms on FPGAs in a few steps.
- Optimized the design workflow by analyzing optimal HLS primitives and easy customization of DP algorithms by the user without hardware re-design from scratch.
- Achieved **32x speedup** and **20x faster implementation time** on FPGAs with similar accuracy to state-of-the-art implementations.
- **Developed** ROADIES, an open-sourced first-of-its-kind tool to infer large-scale phylogenetic trees directly from raw-genomic datasets.

- Designed an optimized genomic workflow, resulting in a **176x speedup** in tree generation, thus reducing computational cost and time for evolutionary genomics research.
- Collaborated with the VGP team from UCSC and evolutionary biologists from Zhejiang University, China, to address their computational bottlenecks.
- Prepared and submitted the manuscript to **Nature Methods** (under review).

Selected Publications [Google Scholar]

- Y. Cao*, **A. Gupta***, J. Liang, Y. Turakhia, "DP-HLS: A high-level synthesis framework for accelerating dynamic programming algorithms in bioinformatics", arXiv 2024. [paper] (* - Co-authors)
- **A. Gupta**, S. Mirarab, Y. Turakhia, "Accurate, scalable, and fully automated inference of species trees from raw genome assemblies using ROADIES", bioRxiv 2024. [paper]
- P. Niemann, **A. Gupta**, R. Drechsler, "T-depth Optimization for Fault-Tolerant Quantum Circuits", IEEE ISMVL 2019. [paper]

Projects

Optimization of HLS4ML Library | *Vitis HLS, Vivado, Git, Python* **April 2023 – June 2023**

- Improved HLS4ML library for efficient Machine Learning hardware inference via High-Level Synthesis.
- Partnered with CERN's HLS4ML team to add some feature enhancements and optimizations.

Parallelized Suffix Array Construction | *C++, CUDA, Git* **January 2023 – March 2023**

- Implemented CUDA-based Suffix Array construction on GPUs, achieving 86-571x speedup compared to CPU baseline.

Parallelized Read Mapping Algorithms | *C++, CUDA, Intel TBB, Git* **January 2023 – March 2023**

- Utilized Intel Thread Building Blocks for bioinformatics read mapping, achieving a significant speed boost.
- Integrated CUDA in read mapping algorithms, streamlining genomic data processing.

Matrix Multiplication Acceleration | *CUDA, MPI, C, Intel AVX2* **October 2022 – December 2022**

- Accelerated C-based matrix multiplication by implementing blocking and Intel AVX2 vectorization.
- Implemented CUDA-based matrix multiplication on K80 and T4 GPUs using blocking and shared memory techniques.
- Optimized Aliev-Panfilov solver performance with C++ and MPI on the Expanse supercomputer, achieving significant computational efficiency gains.

Branch Predictor | *C, Git* **October 2022 – December 2022**

- Developed Gshare, Tournament, Perceptron, and TAGE branch predictors in C, improving CPU branch prediction accuracy.
- Designed L1 Cache with FIFO replacement, optimizing memory access and CPU performance.

Relevant Coursework

- Principles of Computer Architecture
- Parallel Computer Architecture
- Parallel Computation
- Parallel Computation in Bioinformatics
- Design Automation and Prototyping
- Validation and Testing in Embedded Systems
- Algorithms in Computational Biology
- Computational Evolutionary Biology