Anshu Gupta

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Research Interests

Bioinformatics, Hardware accelerators, High-Performance Computing

Education

University of California, San Diego — La Jolla, California
- *Ph.D. student in Computer Science and Engineering, GPA 4.00/4.00 (ongoing)* — *September 2022 – Present*
  Supervisor: Prof. Yatish Turakhia

Indian Institute of Engineering Science and Technology, Shibpur — Howrah, India
- *B.Tech. in Electronics and Telecommunication Engineering; GPA: 9.55/10.0* — *July 2015 – May 2019*
  Supervisor: Prof. Ankita Pramanik

Research Experience

- **University of California, San Diego** — La Jolla, California
  Graduate Student Researcher — *November 2022 - Present*
  - Developing a flexible hardware accelerator for various sequence alignment algorithms using High-level Synthesis.
  - Enhancing FPGA resource utilization by optimizing sequence alignment algorithms, boosting computational efficiency.
  - Developing a software pipeline to deduce species phylogeny from raw genomic sequences, contributing to evolutionary biology insights.
  - Mentoring a team of 3 undergraduate students across two ongoing collaborative projects.
- **Indian Institute of Engineering Science and Technology, Shibpur** — Howrah, India
  Undergraduate Thesis — *August 2018 - April 2019*
  - Developed a specialized model using Convolutional Neural Networks to localize fatal organs in surgical video frames.
  - Utilized TensorFlow to refine network settings, resulting in an accuracy of 92%.
- **University of Bremen** — Bremen, Germany
  DAAD Working Internship in Science and Engineering — *May 2018 - July 2018*
  - Optimized fault-tolerant quantum circuits by reducing its synthesis cost using Clifford+T gate library.
  - Significantly reduced the T-gate count by 10-50%, optimizing quantum circuit synthesis for cost-effectiveness.

Work Experience

- **Analog Devices** — Wilmington, Massachusetts
  ASIC BU Digital Design Intern — *June 2023 - Sep 2023*
  - Working on architectural benchmarking of Cadence Tensilica Xtensa configurable processors.
  - Responsible for characterizing the performance, power and area of configurable processors and optimizing the best configuration for low-power embedded AI applications.
- **Analog Devices** — Bengaluru, India
  Digital Design Engineer — *July 2019 - July 2022*
  - Worked on the development of a scalable digital processing platform.
  - Responsible for architectural evaluation of ARM Cortex-M processor and integration of industry-standard modules.
  - Worked on SRAM and ROM memory generation and integration into SoC using memory compilers.
  - Contributed to Digital Front-end Design and tape-out of Battery Management Systems (BMS) SoC.
  - Ensured quality through tasks such as Lint, Clock/Reset Domain Crossing, and Logic Equivalence Check for RTL design.
  - Optimized Radar Signal Processing algorithms on DSP core and FFT HW accelerator for Automotive Radar Design.
  - Employed SIMD operations to vectorize and evaluate code, reducing cycle counts of the DSP core.

Publications

Object Detection in Surgical Videos Using Neural Networks (2020) | paper
Amit Kumar, Anshu Gupta, Ankita Pramanik
Smart Trends in Computing and Communications: Proceedings of SmartCom 2020, 345–353.

T-depth Optimization for Fault-Tolerant Quantum Circuits (2019) | paper
Philipp Niemann, Anshu Gupta, Rolf Drechsler
2019 IEEE 49th International Symposium on Multiple-Valued Logic (ISMVL).

Projects

- **Parallel Computing in Bioinformatics**
  Supervisor: Prof. Yatish Turakhia
  - Accelerated the Suffix Array construction using various vectorization and parallelization techniques in CUDA.
  - Accelerated the read mapping algorithm in bioinformatics using Intel Thread Building Blocks Library and CUDA.
- **Parallel Computing**
  Supervisor: Prof. Bryan Chin
  - Accelerated matrix multiplication in C using blocking and vectorization on Intel AVX2.
  - Accelerated matrix multiplication in CUDA using blocking and shared memory on K80 and T4.
  - Accelerated Aliev-Panfilov solver using C++, MPI on Expanse supercomputer.
- **Modelling Branch Predictor and L1 Cache Simulator**
  Supervisor: Prof. Jishen Zhao
  - Modelled various branch predictors like Gshare, Tournament, Perceptron, TAGE, and L1 Cache structure with FIFO replacement in C.
- **Design Automation of Embedded Systems**
  Supervisor: Prof. Ryan Kastner
  - Enhanced the HLS4ML library which optimizes the workflow of Machine Learning hardware inference using High-Level Synthesis.
  - Collaborated with HLS4ML development team in CERN to work on the enhancement features.

Awards and Fellowships

- Secured **UCSD CSE departmental fellowship** for first year of PhD program.
- Secured university rank **4** in the entire undergraduate batch of IIEST Shibpur in 2019.
- Selected as **DAAD WISE Scholar** for pursuing summer internship at **University of Bremen** in 2018.

Technical Skills

- **Languages** Verilog, SystemVerilog, C, C++, R, Python, MATLAB, Embedded C, CUDA, Intel TBB.
- **Tools** Synopsys SpyGlass, Cadence Conformal, Cadence SimVision, Synopsys Memory Compiler, Vitis HLS, TensorFlow, Snakemake.
- **Protocols** SPI, QSPI, I2C, UART, DMA, CAN, JTAG, SWD, ARM CoreSight, ARM AMBA protocols.

Relevant Courses

- Principles of Computer Architecture (CSE 240A)
- VLSI and CAD
- Digital Signal Processing
- Parallel Computer Architecture (CSE 240B)
- Parallel Computation (CSE 260)
- Integrated Circuits and Systems
- Parallel Computing in Bioinformatics (CSE 284)
- Design Automation and Prototyping of Embedded Systems (CSE 237D)